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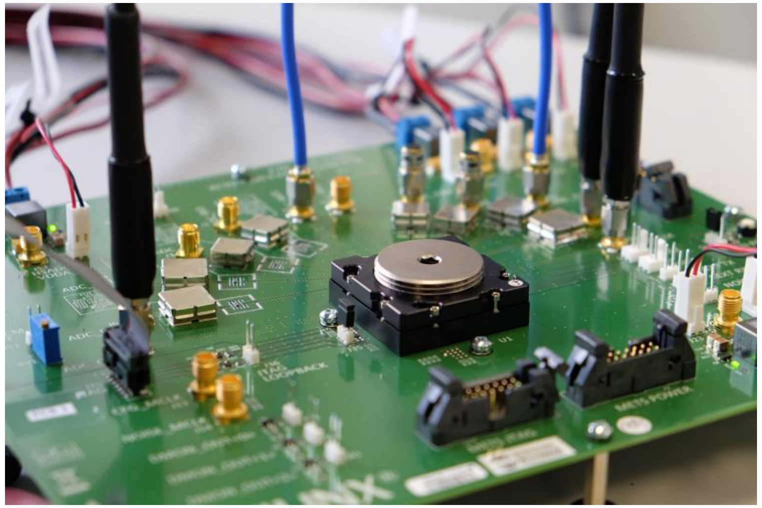
22nd August 2017

Xilinx RFSoC - Monolithic Integration of RF Data Converters with All Programmable SoC in 16nm FinFET for Digital-RF Communications

Brendan Farley, Senior Director, Analog & Digital-RF

Agenda

- In Wireless, RF Data Converters are the new SERDES
- RF in the Digital Domain
- RFSoC Overview
- Applications



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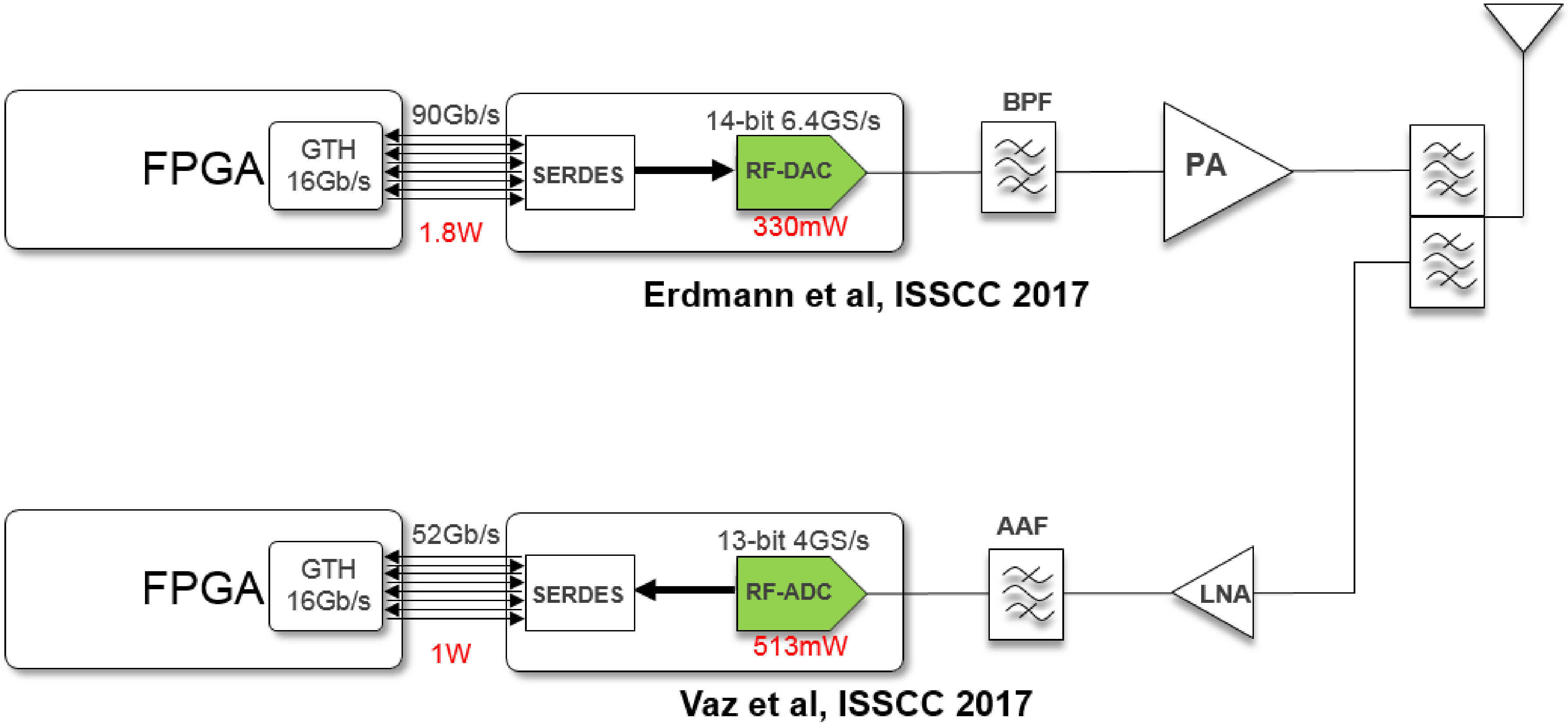
In Wireless, RF Data Converters are the new SerDes

RF Data Converter Overview

- State of the at RF Data Converters
  - RF-ADC
  - RF-DAC



- Interface power dominates
  - The limiting factor in many multi-channel systems

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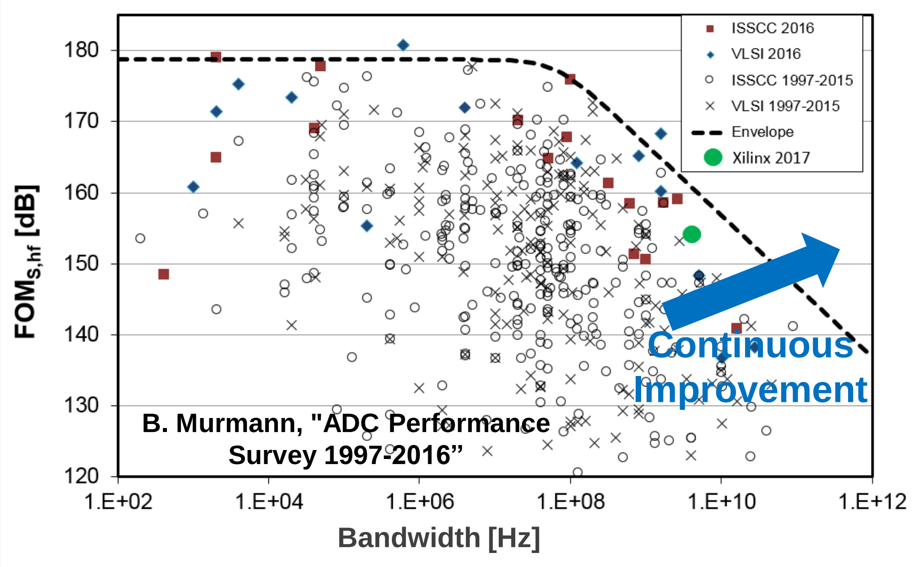
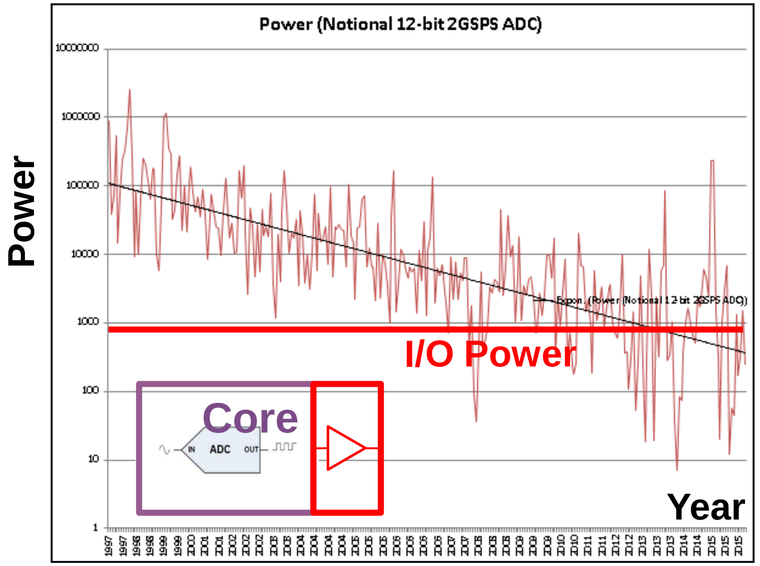
Future trends in RF Data Converters



- Continuous power efficiency improvements
- Sampling rates extending to multi-GHz

- Digital I/O bandwidth increasing
- I/O power not scaling
- Integration removes the bottleneck
  - The new SERDES for wireless



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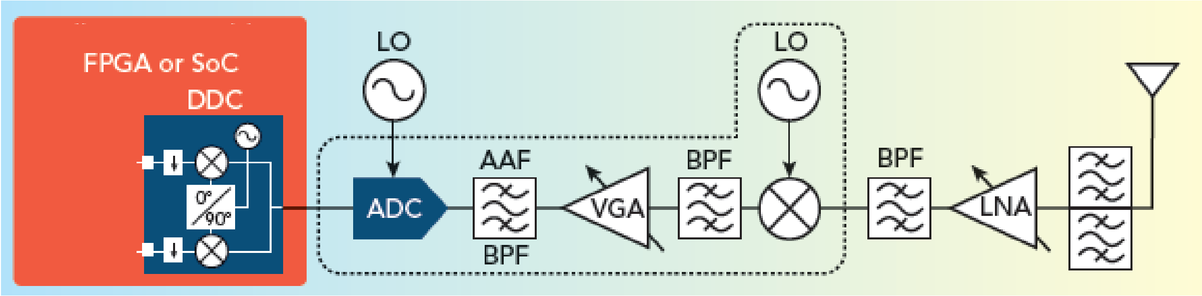
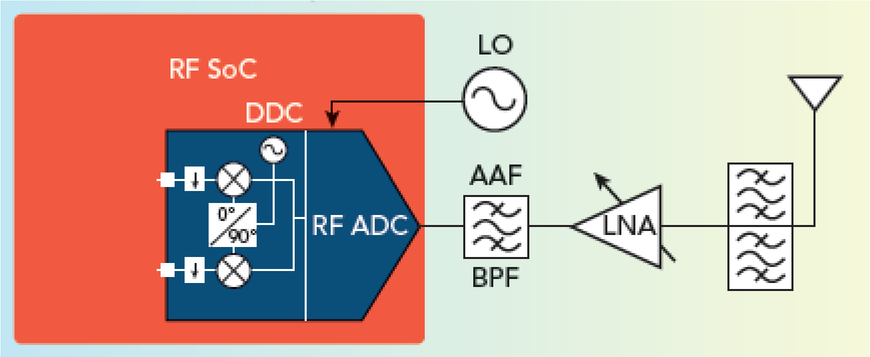
RF in the Digital Domain

Analog versus Digital RF Architectures

- **Analog RF**
  - Custom analog, narrow-band
  - Expensive in size, power and cost
  - Relaxed data converter specs e.g. 500MS/s



- **Digital RF**
  - Flexible, low power, wide-band
  - Lower size, power and system cost
  - Demanding RF data converter specs e.g. 6.4GS/s



FinFET Technology
Enabling Viable Digital-RF Implementation

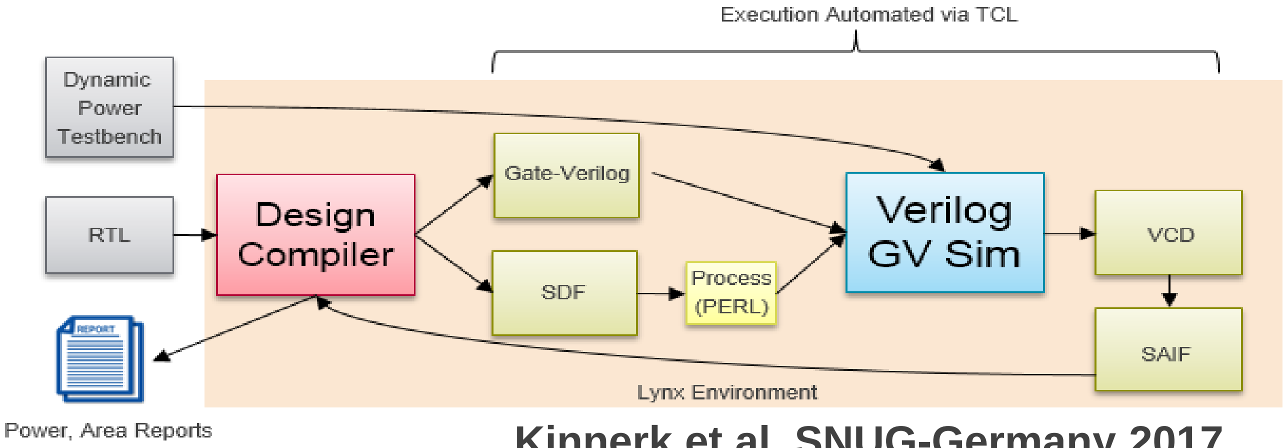
- **Excellent analog transistor characteristics**
  - Wideband RF sampling switches
  - High speed comparators, amplifiers and clocking circuits
  - Some challenges: low power supply, isolation from digital

- **Excellent digital logic characteristics**
  - Cost and power efficient digitally assisted analog calibration logic
    - 150K logic gates for calibration of each 4GS/s ADC
  - Fast, low cost, low power digital-RF functionality
  - Some challenges: digital / analog verification, power integrity

- **Digital implementation in 16nm FinFET vs. 65nm**
  - 10x area reduction
  - 4x power reduction

RFSoC
Power Integrity

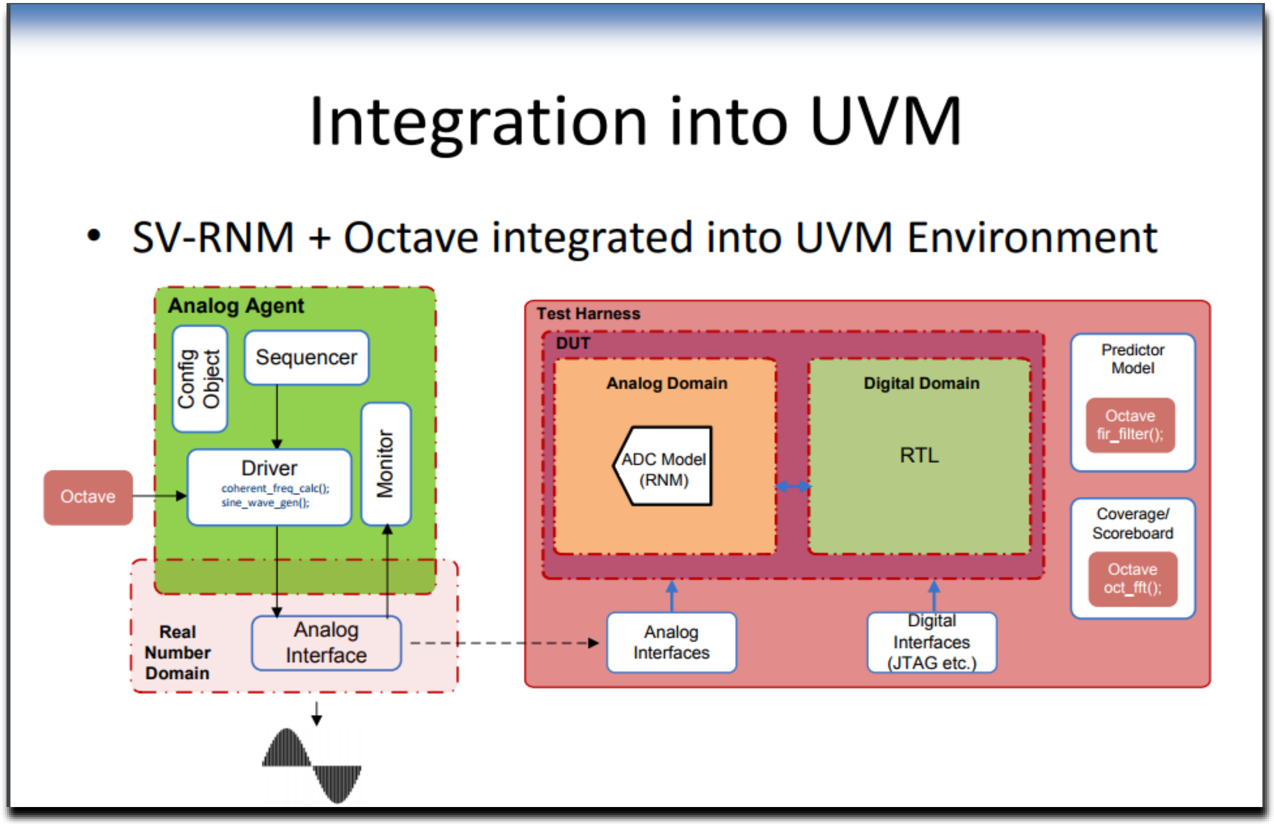
- **1.5M Instance RF SoC synthesis QoR w/ Fmax >1GHz**
- **13 layer metal stack with high resistance lower metals**
  - EMIR closure
  - Power supply noise
- **Digital dynamic power optimization critical**
  - Glitch power >25% total
- **Custom flow illustrated used to achieve ~25% power reduction**



Kinnerk et al, SNUG-Germany 2017

RFSoC
Analog / Digital Verification

- Validate digital calibration of analog circuits over 1000's of cycles / samples
- Netlist Real Number Models (RNMs) from analog schematics
  – Model at lowest feasible level
  – Validate RNM using co-sim
- Performance
  – Closed loop calibration of complex analog circuit
    - SV-RNM of 16 parallel blocks takes 5 minutes
    - Co-sim of 1 block takes 18 hours

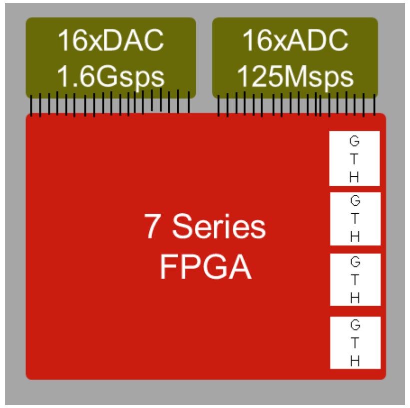


McGrath et al, DVCon Europe 2015

RFSoC Overview

Towards Digital-RF Integration

1st Generation

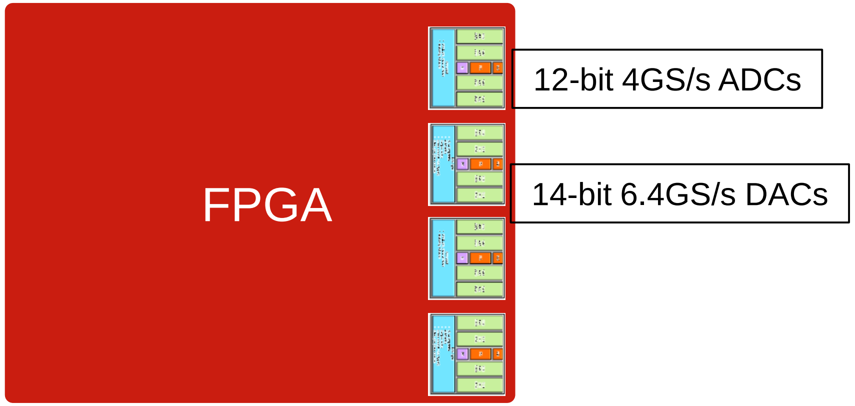


- Si interposer w/ TSV – 65nm analog / 28nm digital
- 12-bit 500MS/s ADCs, 14-bit 1.8GS/s DACs
- 1mW per MS/s

ISSCC 2014 / SESSION 6

6.3 A Heterogeneous 3D-IC Consisting of Two 28nm FPGA Die and 32 Reconfigurable High-Performance Data Converters
C. Erdmann[1], D. Lowney[1], A. Lynam[1], A. Keady[1], J. McGrath[1], E. Cullen[1], D. Breathnach[1], D. Keane[1], P. Lynch[1], M. De La Torre[1], R. De La Torre[1], P. Lim[1], A. Collins[1], B. Farley[1], L. Madden[2]
[1]Xilinx, Dublin, Ireland
[2]Xilinx, San Jose, CA

RFSoC



- Monolithic Single Die - 16nm FinFET
- 12-bit 4GS/s ADCs, 14-bit 6.4GS/s DACs
- 100µW per MS/s, 20x per MS/s area reduction

International Solid-State Circuits Conference | February 5–9, 2017 | San Francisco, CA

SESSION 16 **Tuesday February 7th, 1:30 PM**

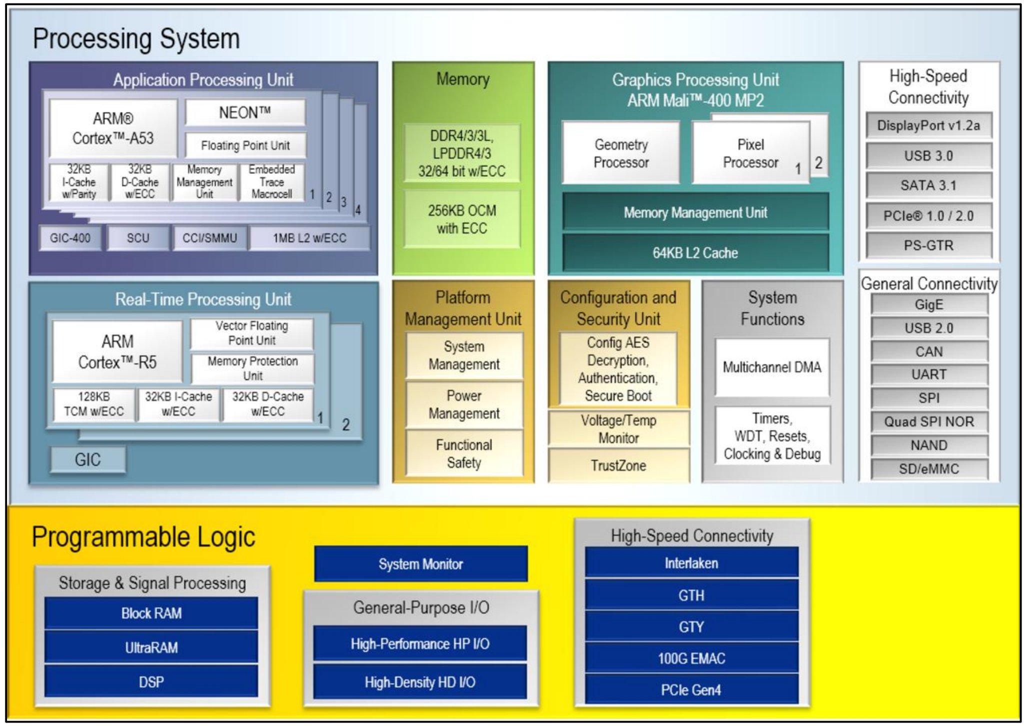
Gigahertz Data Converters
Session Chair: *Jan Mulder, Broadcom, Bunnik, The Netherlands*
Associate Chair: *Paul Ferguson, Analog Devices, Wilmington, MA*

1:30 PM
16.1 A 13b 4GS/s Digitally Assisted Dynamic 3-Stage Asynchronous Pipelined-SAR ADC
B. Vaz[1], A. Lynam[1], B. Verbruggen[1], A. Laraba[2], C. Mesadri[1], A. Boumaalif[2], J. Mcgrath[3], U. Kamath[1], R. D. L. Torre[1], A. Manlapat[1], D. Breathnach[3], C. Erdmann[1], B. Farley[1]

2:30 PM
16.3 A 330mW 14b 6.8GS/s Dual-Mode RF DAC in 16nm FinFET Achieving -70.8dBc ACPR in a 20MHz Channel at 5.2GHz
C. Erdmann, E. Cullen, D. Brouard, R. Pelliconi, B. Verbruggen, J. Mcgrath, D. Collins, M. De La Torre, P. Gay, P. Lynch, P. Lim, A. Collins, B. Farley

RFSoC
Resources & Performance

- Device requirements
  - Maximise programmable DSP bandwidth per channel
  - <35W for passive cooling
  - Processor for ease of use and co-efficient calcs
  - Wideband serial interface to baseband
- 32Gb/s GTY SerDes
- Programmable Logic
  - High densities of DSP slice and system logic cells
- Processor sub-system
  - Quad-core ARM A53 @1.5GHz
  - Dual-core R5 'Real-Time' Processing Units



Operating Voltage (V_{CCINT})	1V 7 Series (28nm) V_{NOM}	0.95V UltraScale (20nm) V_{NOM}	0.85V UltraScale+ (16nm) V_{NOM}	0.72V UltraScale+ (16nm) V_{LOW}
Normalized Fabric Performance	1.0x	1.2x	1.6x	1.2x
Normalized Total Power	1.0x	.7x	.8x	.5x
Performance/Watt	1.0x	1.7x	2x	2.4x

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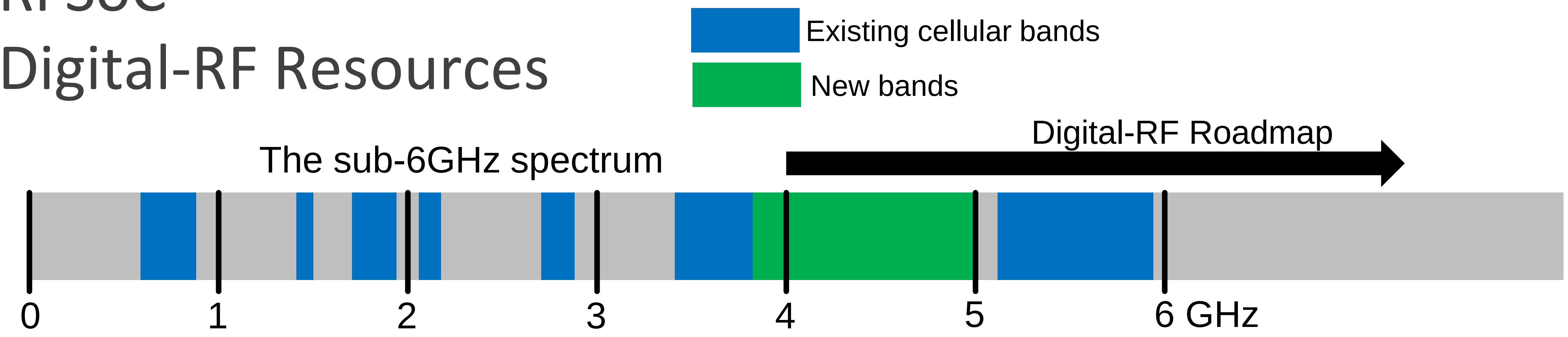
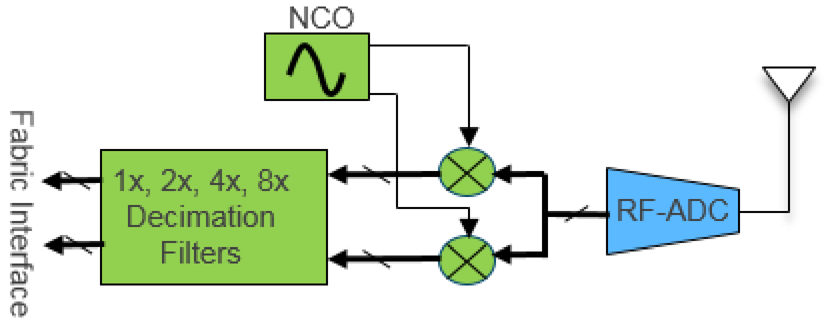
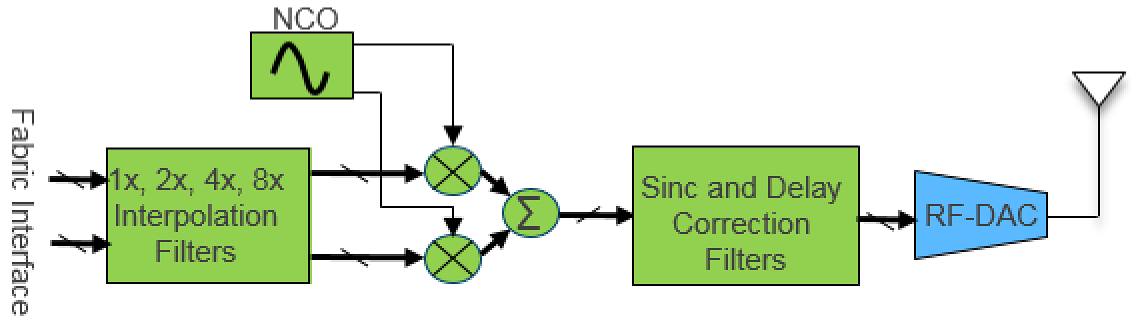
RFSoC
Digital-RF Resources



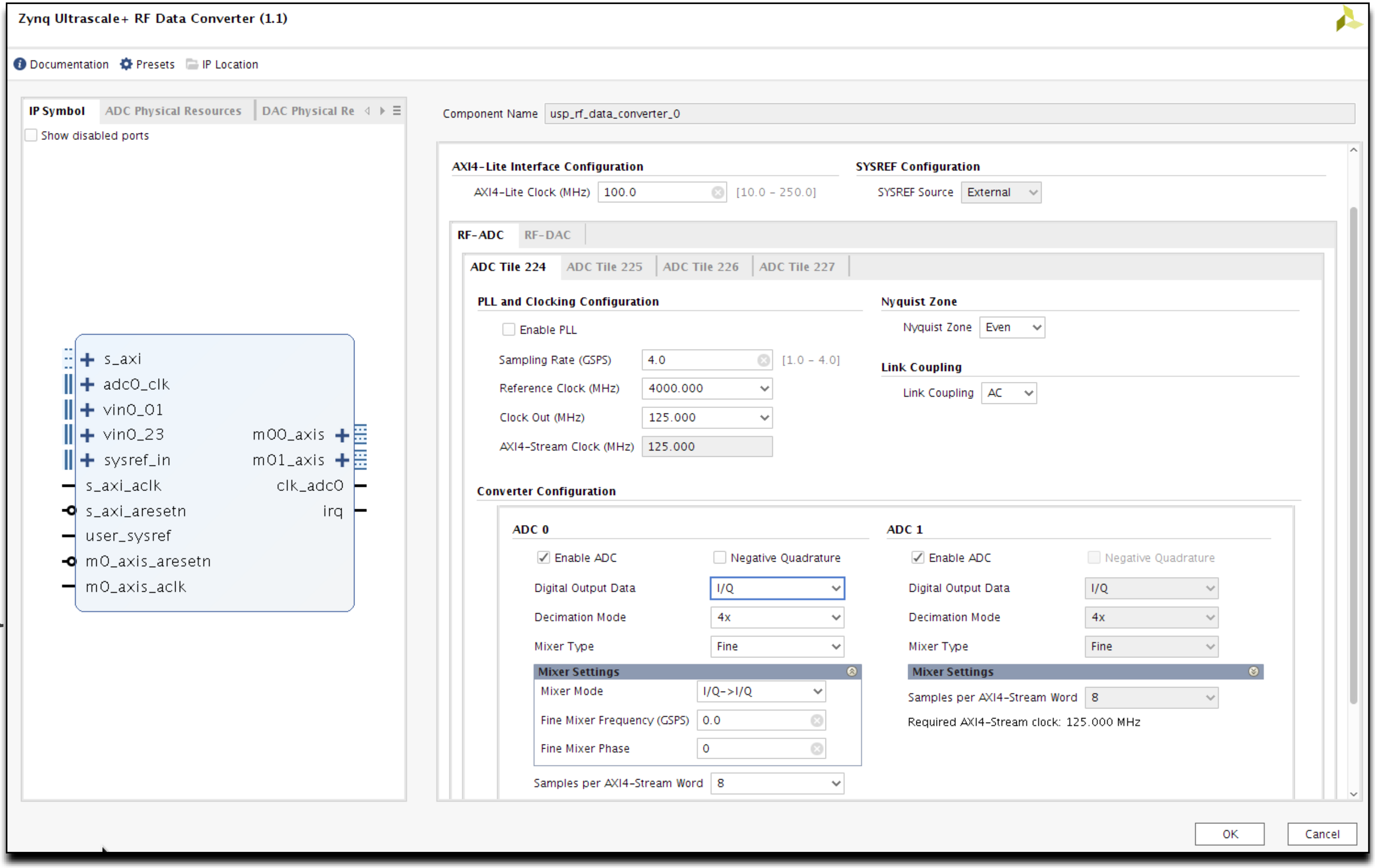
- Arrays of 6.4GS/s DACs and 4GS/s ADCs
- Integrated low phase noise PLL
- Full Complex Mixers
  - 48-bit NCO per DAC / ADC
- 1x, 2x, 4x, 8x Interpolation and Decimation
- Quadrature Modulator Correction
- Sinx/x and Delay Correction Filters
- Flexible FPGA fabric interface





RFSoC
RF Configuration Tools & Programming

- Configuration Wizard for initial settings
- Linux drivers for runtime setting adjustments
- AXI4-Lite for configuration
- AXI4-Stream for data interface to fabric



RFSoC Applications

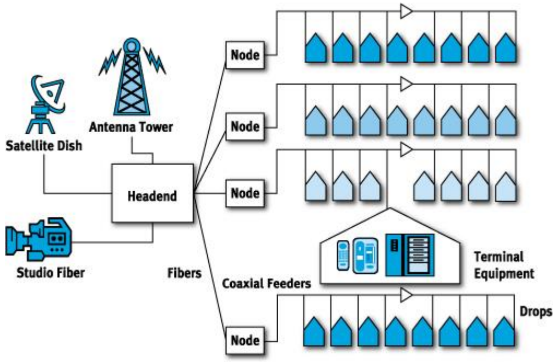
RFSoC Applications

Primary

Wireless backhaul

Radio

Cable Remote PHY



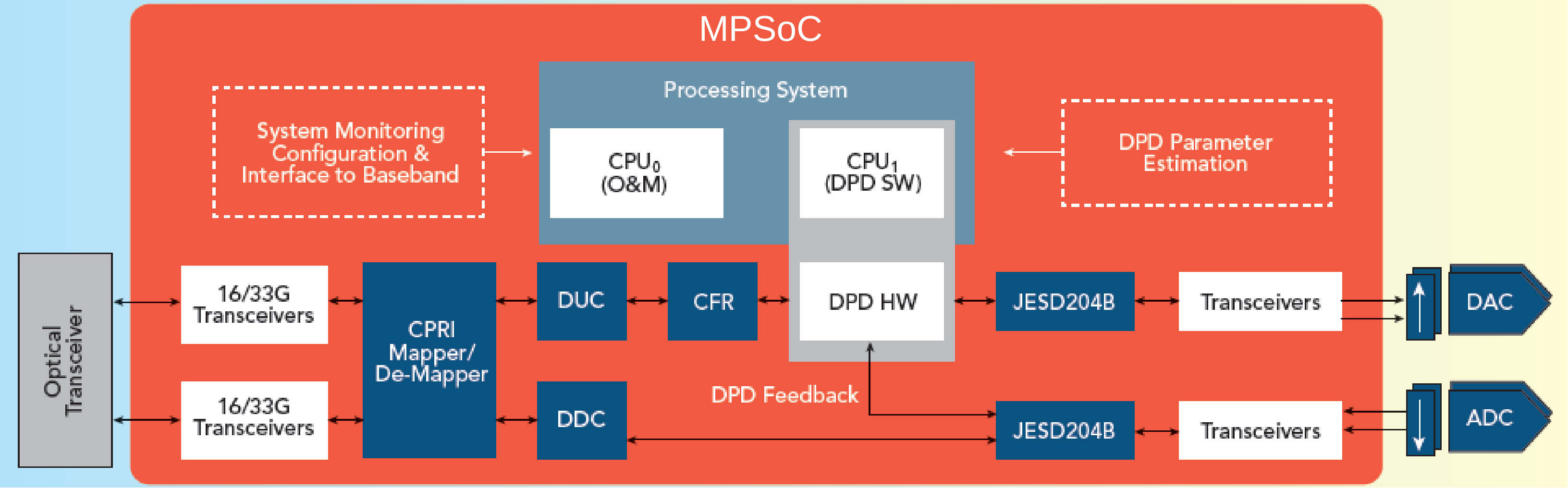
Secondary

Test and Measurement

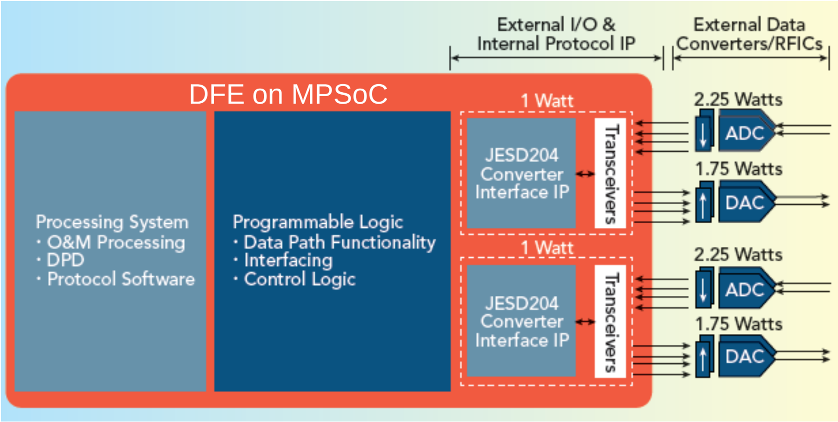
Imaging (Security / Medical)

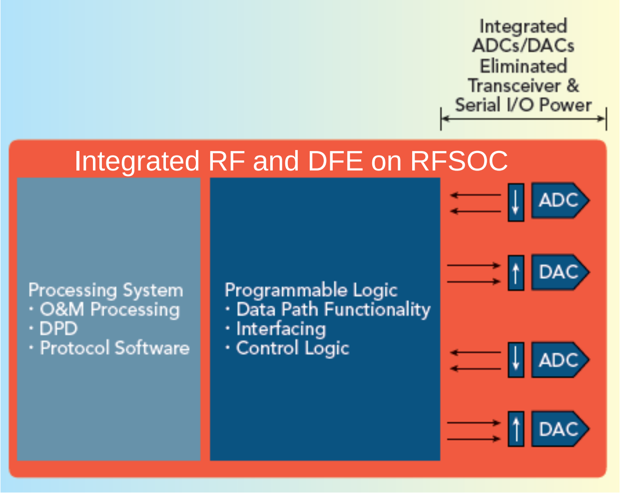
A&D Radars

RFSoC Applications
Basestation Remote Radio Head (1)



- MPSoC -> RFSoC





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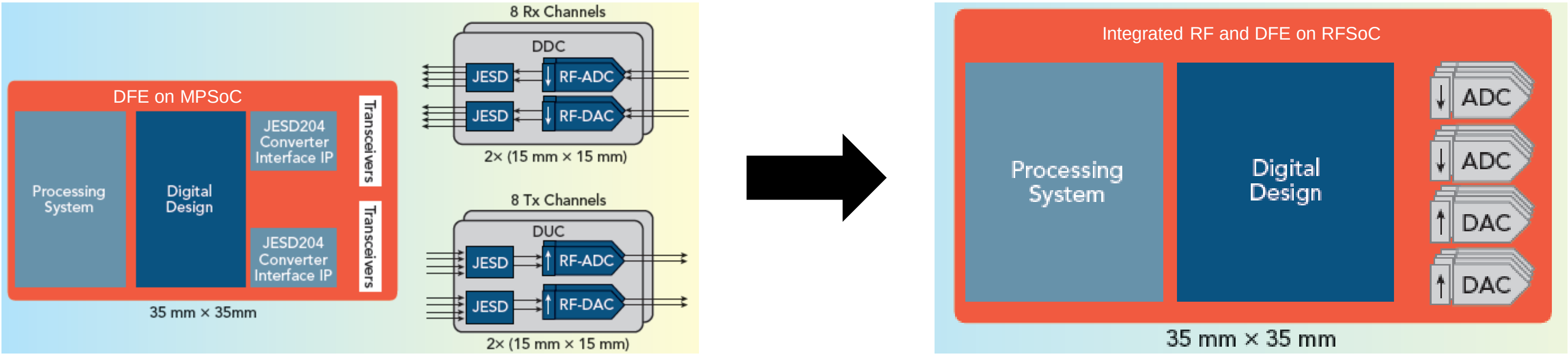
RFSoC Applications
Basestation Remote Radio Head (2)

- Power Reduction
  - Optimised 16nm data converter cores
  - Eliminated SerDes interface
  - 27 W RFSoC versus 55 W discrete

POWER SAVINGS IN DIGITAL RADIO (WITH DPD) USING AN INTEGRATED SUBSYSTEM			
	4x4 100 MHz	4x4 200 MHz	8x8 100 MHz
Discrete Implementation			
Programmable Device	15 W	23 W	23 W
ADC/DAC Components	16 W	16 W	32 W
TOTAL POWER	**31 W**	**39 W**	**55 W**
Integrated RF-Analog			
Programmable Device + RF Subsystem	18 W	25 W	27 W
TOTAL POWER SAVINGS	**41%**	**37%**	**51%**

- Form Factor Reduction



Collins et al, Microwave Journal, June 2017

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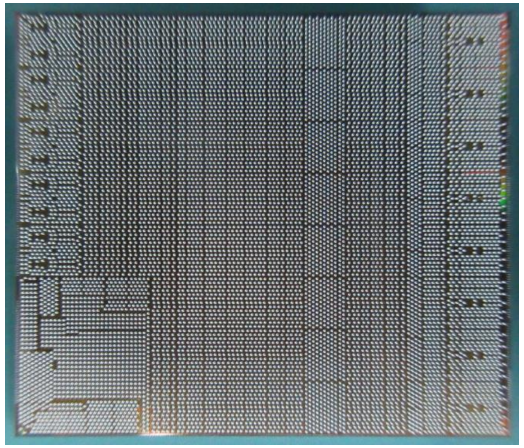
RFSoC Concluding Remarks

- RF data converter integration enables migration of functions from the analog to the digital domain
  - Flexibility, power efficiency, low system cost, weight and size
- FinFET technology simultaneously supports excellent RF performance and high density, power efficient digital functionality
- RFSoC offers a digital solution for a broad set of markets
  - Wireless, Wired, T&M, Radar, Imaging
- Digital integration, # channels and power reduction will drive migration to <16nm



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